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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,458	03/24/2006	Koji Otsuka	SHG-046P2-319/OSP-19842	2611
26875 7590 05/14/2008 WOOD, HERRON & EVANS, LLP 2700 CAREW TOWER 441 VINE STREET CINCINNATI, OH 45202				
EXAMINER				
ROLAND, CHRISTOPHER M				
ART UNIT		PAPER NUMBER		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/573,458

**Applicant(s)**

OTSUKA ET AL.

**Examiner**

CHRISTOPHER M. ROLAND

**Art Unit**

2814

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date 03/24/06
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Examiner notes that Applicant's claim to foreign priority in Japanese Patent Application 2004-289248 does not provide support for the embodiment found in FIG. 8 of Applicant's disclosure.

### ***Drawings***

2. Figure 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

III-V NITRIDE SEMICONDUCTOR DEVICE COMPRISING A CONCAVE  
SCHOTTKY CONTACT AND A CONCAVE OHMIC CONTACT.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation, "a first concave portion ... that faces the interface between the first semiconductor layer and the second semiconductor layer." It is unclear from the disclosure how the concave portion faces the interface, what surface faces the interface, or how the concave portion may face the interface even as it extends deeper than said interface.

Claim 2 recites the limitation, "wherein the first electrode ... is formed so as to face the two-dimensional carrier." It is unclear from the disclosure how the first electrode faces the two-dimensional carrier or how the first electrode may face the two-dimensional carrier even as it extends deeper than said two-dimensional carrier.

Claim 3 recites the limitation, "a first concave portion ... that faces the interface between the third semiconductor layer and the second semiconductor layer." It is unclear from the disclosure how the concave portion faces the interface, what surface

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faces the interface, or how the concave portion may face the interface even as it extends deeper than said interface.

Claims 1-7 recite the limitation, "as far as." It is unclear from the disclosure whether, "as far as," is to be interpreted as, "at least as far as," "only as far as," "precisely as far as," "substantially as far as," or some other language to distinctly claim relative distances among the claimed features.

Claim 8 recites the limitation, "the second electrode is formed so as to sandwich and face the first electrode." It is unclear from the disclosure how the second electrode faces the first electrode.

Claims 9 and 10 are rejected for merely containing the flaw(s) of the parent claims.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 2, and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Margalit et al. (US Patent 4,636,823, hereinafter Margalit '823).

With respect to claim 1, Margalit '823 teaches (FIG. 4) a semiconductor device as claimed, comprising:

a first semiconductor layer (14) that is formed from a first semiconductor material (col. 5, ln. 21-45);

a second semiconductor layer (16') that is formed from a second semiconductor material on the first semiconductor layer (col. 5, ln. 21-45);

a two-dimensional carrier that is formed within the first semiconductor layer and in the vicinity of an interface between the first semiconductor layer and the second semiconductor layer (col. 5, ln. 21-45);

a first concave portion that is formed extending from a primary surface of the second semiconductor layer that faces the interface between the first semiconductor layer and the second semiconductor layer as far as the interface (col. 5, ln. 21-45);

a first electrode (18) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction between the first and second semiconductor layers (col. 3, ln. 23-28; col. 5, ln. 21-45); and

a second electrode (20) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (col. 3, ln. 23-28; col. 5, ln. 21-45).

With respect to claim 2, Margalit '823 teaches wherein the first electrode is formed so as to extend from the primary surface of the second semiconductor layer as far as the two-dimensional carrier, or is formed so as to face the two-dimensional carrier and separated therefrom by a distance that allows a quantum mechanical tunnel effect to be obtained (col. 5, ln. 21-45).

With respect to claim 10, Margalit '823 teaches wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion (col. 5, ln. 21-45).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-5 and 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzawa et al. (US Patent 4,772,925, hereinafter Fukuzawa '925) in view of Margalit '823.

With respect to claim 1, Fukuzawa '925 teaches (FIG. 3A) a semiconductor device substantially as claimed, comprising:

a first semiconductor layer (2) that is formed from a first semiconductor material (col. 2, ln. 29 – col. 5, ln. 39);

a second semiconductor layer (4) that is formed from a second semiconductor material on the first semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a two-dimensional carrier that is formed within the first semiconductor layer and in the vicinity of an interface between the first semiconductor layer and the second semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a first concave portion that is formed extending from a primary surface of the second semiconductor layer that faces the interface between the first semiconductor layer and the second semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a first electrode (6) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction between the first and second semiconductor layers (col. 2, ln. 29 – col. 5, ln. 39); and

a second electrode (5 and 7) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39).

Thus, Fukuzawa '925 is shown to teach all the features of the claim with the exception of wherein said first concave portion is formed extending as far as the interface.

However, Margalit '823 teaches a gate (18) recessed to an interface between two semiconductor layers having different bandgaps and forming a schottky junction between said two semiconductor layers (col. 5, ln. 21-45) to reduce source and drain parasitic resistance (col. 3, ln. 29-32) and to optimize important parameters such as breakdown voltage (col. 5, ln. 43-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the first concave portion of Fukuzawa '925 extending as far as the interface as taught by Margalit '823 to reduce source and drain parasitic resistance and to optimize important parameters such as breakdown voltage.



With respect to claim 2, Margalit '823 teaches wherein the first electrode is formed so as to extend from the primary surface of the second semiconductor layer as far as the two-dimensional carrier, or is formed so as to face the two-dimensional carrier and separated therefrom by a distance that allows a quantum mechanical tunnel effect to be obtained (col. 3, ln. 66 – col. 5, ln. 7).

With respect to claim 3, Fukuzawa '925 teaches (FIG. 3B) a semiconductor device substantially as claimed, comprising:

a first semiconductor layer (2) that is formed from a first semiconductor material (col. 2, ln. 29 – col. 5, ln. 39);

a second semiconductor layer (4) that is formed from a second semiconductor material on the first semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a third semiconductor layer (4') that is sandwiched between the first semiconductor layer and the second semiconductor layer and that is formed having a thickness that allows a quantum mechanical tunnel effect to be obtained (col. 2, ln. 29 – col. 5, ln. 39);

a two-dimensional carrier that is formed within the first semiconductor layer and on the third semiconductor layer side of the first semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a first concave portion that is formed extending from a primary surface of the second semiconductor layer that faces the interface between the third semiconductor layer and the second semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39);

a first electrode (6) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction between the first and second semiconductor layers (col. 2, ln. 29 – col. 5, ln. 39); and

a second electrode (5 and 7) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (col. 2, ln. 29 – col. 5, ln. 39).

Thus, Fukuzawa '925 is shown to teach all the features of the claim with the exception of wherein said first concave portion is formed extending as far as the interface.

However, Margalit '823 teaches a gate (18) recessed to an interface between two semiconductor layers having different bandgaps and forming a schottky junction between said two semiconductor layers (col. 5, ln. 21-45) to reduce source and drain parasitic resistance (col. 3, ln. 29-32) and to optimize important parameters such as breakdown voltage (col. 5, ln. 43-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the first concave portion of Fukuzawa '925 extending as far as the interface as taught by Margalit '823 to reduce source and drain parasitic resistance and to optimize important parameters such as breakdown voltage.

With respect to claim 4, Fukuzawa '925 teaches wherein there is further provided a second concave portion that is formed extending from the primary surface of the second semiconductor layer as far as the interface between the first semiconductor layer and the second semiconductor layer, and wherein the second electrode is formed on a bottom surface and side surface of the second concave portion (col. 2, ln. 29 – col. 5, ln. 39).

With respect to claim 5, Fukuzawa '925 teaches wherein there is further provided a second concave portion that is formed extending from the primary surface of the second semiconductor layer as far as the interface between the third semiconductor layer and the second semiconductor layer, and wherein the second electrode is formed on a bottom surface and side surface of the second concave portion (col. 2, ln. 29 – col. 5, ln. 39).

With respect to claim 8, Fukuzawa '925 teaches wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to sandwich and face the first electrode (col. 2, ln. 29 – col. 5, ln. 39).

With respect to claim 9, Fukuzawa '925 teaches wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to surround the first electrode (col. 2, ln. 29 – col. 5, ln. 39).

With respect to claim 10, Margalit '823 teaches wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion (col. 5, ln. 21-45).

7. **Claims 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzawa '925 and Margalit '823 as applied to claims 1-3 above, and further in view of Patel et al. (UK Patent Application Publication 2 279 806, hereinafter Patel '806).

With respect to claims 6 and 7, Fukuzawa '925 and Margalit '823 teach the device as described in claims 1-3 including the additional limitation wherein the second electrode is formed on the bottom surface and side surface of the second concave portion (Fukuzawa '925, col. 2, ln. 29 – col. 5, ln. 39).

Thus, Fukuzawa '925 and Margalit '823 are shown to teach all the features of the claim with the exception of wherein the second electrode is formed so as to extend from the primary surface of the second semiconductor layer as far as the two-dimensional carrier; and wherein there is further provided a second concave portion that is formed extending from the primary surface of the second semiconductor layer as far as the two-dimensional carrier, and wherein the second electrode is formed so as to extend from the primary surface of the second semiconductor layer as far as the two-dimensional carrier.

However, Patel '806 teaches forming ohmic contact layers (33) extending beyond the interface of two semiconductor layers as far as the 2DEG (15) (p. 7, ln. 21—p. 8, ln. 24) in a method to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device (p. 5, ln. 12-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode disposed in the

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second concave portion of Fukuzawa '925 and Margalit '823 as far as the two-dimensional carrier as taught by Patel '806 to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Wolter (US Patent 4,677,457);

Ando (US Patent 5,105,241);

Sheppard et al. (US Patent Application Publication 2006/0019435);

Machida et al. (US Patent Application Publication 2007/0228401);

Ueno et al. (US Patent Application Publication 2007/0284653);

Murata et al. (US Patent Application Publication 2005/0139838);

Takada (Japanese Patent Application Publication 2001-102565);

Imamura et al. (Japanese Patent Application Publication 62-213279); and

Hwang (US Patent Application Publication 2005/0263789) teach III-V nitride semiconductor devices comprising schottky and ohmic contacts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER M. ROLAND whose telephone number is (571)270-1271. The examiner can normally be reached on Monday-Friday, 8:00AM-5:00PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. M. R./  
Examiner, Art Unit 2814

/Anh D. Mai/  
Primary Examiner, Art Unit 2814